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# ENVELOPE SWITCHED DOHERTY POWER AMPLIFIER FOR RF APPLICATIONS (PREPRINT)

**Jinseong Jeong and Yuanxun Ethan Wang**

## DECEMBER 2005

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**14. ABSTRACT**
This report was developed under a SBIR contract. A new concept of envelope switched Doherty amplifier is introduced. The proposed amplifier maintains maximum efficiency over a wide range of output power fluctuation. The essential idea is to drive two amplifier devices connected in Doherty configuration with a pulsed envelope signal. A high-Q, low loss filter is placed at the output to recover for linearity and to generate a time-varying equivalent load impedance for optimal efficiency performance. Ideally, for a pair of equally sized and identically biased Class B amplifiers, a maximum efficiency, 78.5%, should be maintained all the way down to the 6dB output back-off level. This concept is demonstrated in the experiment with a pair of GaAs FETs at a frequency of 1.87GHz in the PCS band. A maximum output power of 32.7dBm with a PAE of 46% is measured and a PAE of 34.4% is measured at 6dB back-off level including the filter loss at the power amplifier (PA) output. The proposed architecture can be applied in designing high efficiency PAs with non-constant envelope modulations.

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# Envelope Switched Doherty Power Amplifier for RF Applications

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***Abstract* — A new concept of envelope switched Doherty amplifier is introduced. The proposed amplifier maintains maximum efficiency over a wide range of output power fluctuation. The essential idea is to drive two amplifier devices connected in Doherty configuration with a pulsed envelope signal. A high-Q, low loss filter is placed at the output to recover for linearity and to generate a time-varying equivalent load impedance for optimal efficiency performance. Ideally, for a pair of equally sized and identically biased Class B amplifiers, a maximum efficiency, 78.5%, should be maintained all the way down to the 6dB output back-off level. This concept is demonstrated in the experiment with a pair of GaAs FETs at a frequency of 1.87GHz in the PCS band. A maximum output power of 32.7dBm with a PAE of 46% is measured and a PAE of 34.4% is measured at 6dB back-off level including the filter loss at the power amplifier (PA) output. The proposed architecture can be applied in designing high efficiency PAs with non-constant envelope modulations.***

***Index Terms* — power amplifier, non-constant envelope modulation, pulse switched amplifier, Kahn technique, polar amplifier, Delta-Sigma modulation, High-Q filter, switched resonator, Doherty amplifier.**

## I. Introduction

Conventional linear power amplifiers (PAs) such as Class A and Class AB severely degrade in power efficiency as the highest efficiency cannot be maintained when they are driven by non-constant envelope signals. For this reason, efficiency improvement techniques such as Doherty amplifiers, outphasing and Kahn techniques have been exploited [1]. All of these schemes are intended to operate the PA in saturated mode rather than linear mode as much as possible.

Recently, a new approach of linear power amplification utilizing digitally driven switching amplifier and output filtering was introduced in [2]. This scheme provides well controlled linearity as well as high efficiency. Linearity is preserved by the combination of a linear passive output bandpass filter and sophisticated digital signal processing such as delta-sigma modulations. Theoretically, high efficiency can be achieved by switching amplifiers. However, no suitable switching amplifier scheme other than Class D configuration has been found because of output filter requirements. Due to the switching power loss, Class D PAs are hardly found in RF and microwave applications. In [3] and [4], envelope delta-sigma modulation (EDSM) was proposed to overcome the drawbacks of Class D amplifiers and was first applied in the form of a Kahn transmitter. In EDSM, a delta-sigma modulator modulates the RF input signal envelope instead of modulating the RF input directly. It relaxes the speed requirement of the delta-sigma modulator and also reduces the switching rate below the RF carrier frequency. As described in Fig. 1, a baseband processor generates amplitude and phase. An envelope modulator is used to discretize the envelope signal to rectangular pulses. The phase-modulated carrier is passed to the input of a high efficiency PA. The PA amplifies the carrier signal but under the switching control of the discretized envelope to generate amplitude variation. The original envelope is restored from the output filter which has a high-Q and a low loss. In the Kahn technique, the overall efficiency depends on the efficiency of the envelope modulator and it is hard to make a highly efficient modulator because it has to drive main amplifier's high current drain.

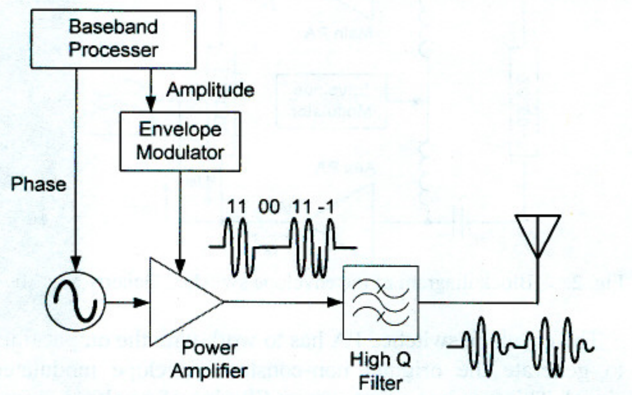


Fig. 1. Block diagram of envelope delta-sigma modulation system.

This paper proposes a new amplifier scheme which is most suitable for the EDSM approach. It is called envelope switched Doherty (ESD) amplifier scheme and it promises maximum efficiency for a wide range of output power level without compromising linearity performance. In this scheme, two amplifiers are connected to each other in a way similar to Doherty amplifiers except that the output is terminated with a high-Q and low loss filter as shown in Fig. 2. Despite this similarity, the operating principle of the ESD amplifier is fundamentally different from that of traditional Doherty amplifiers in the following two aspects. First, in Doherty amplifiers, the main amplifier remains at saturation at a certain range of output power, but the auxiliary amplifier remains at saturation only for two levels of output power, which results in an efficiency dip in the middle range. In the proposed ESD scheme, this problem no longer exists as both

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amplifiers work in saturation mode for up to 6dB output back-off level in the case where identical amplifier devices are used. The range of high efficiency operation can be further extended if asymmetrical pairs of devices are used [5]. Second, Doherty amplifiers intrinsically work in a linear mode which requires accurate control of the bias conditions, the gain characteristics and even the peripheral sizes of the devices in order to achieve linear amplification. These requirements are not necessary in the proposed ESD scheme as both transistors are overdriven to saturation mode and the linearity is controlled by the pulse width modulation duty cycle.

## II. Principle of Operation and Analysis

The ESD amplifier shown in Fig. 2, consists of a pair of FET devices which are connected through quarter-wave impedance transformers. The switched envelope pulses are generated by the envelope modulator. It controls the gates of both devices to turn them on and off simultaneously. A high-Q current filter is placed at the output to prevent sharp change of the current and to restore the original analog envelope.

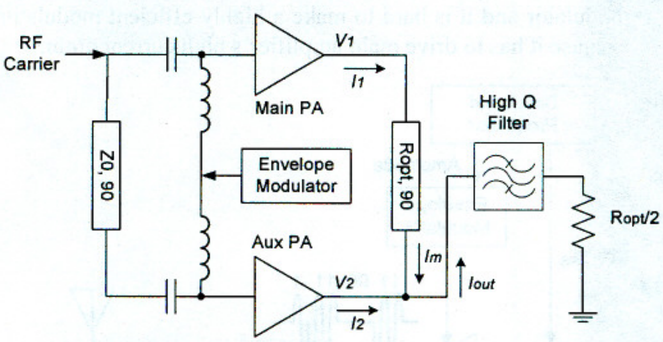


Fig. 2. Block diagram of the envelope switched Doherty amplifier.

The envelope switched PA has to work with the output filter to generate the original non-constant envelope modulated signal. This requires either current filtering of a voltage source or voltage filtering of a current source. This is the reason why only Class D amplifiers could be used with the filter in conventional schemes. Forming a voltage source requires the PA to provide maximum current absorption, e.g., RF short at the input of the filter when envelope modulator output is "0" and well-controlled RF voltage with maximum current output capability when the output is "1" to preserve the linearity of the filtered output. Another necessary attribute of the PA is that the high efficiency needs to be maintained for continuously varying output current levels, which jointly results from the duty cycles of the switching pulses and the filter. Since the output high-Q filter impacts the efficiency behavior of the PA, the PA design has to be carried out with consideration of the filter termination.

The principle of the ESD amplifier consisting of two identical devices is summarized as follows: assuming both devices work in Class B and the maximum drain voltages and current are $V_{max}$ and $I_{max}$. To form "0" state, both devices are turned off and both PAs are open looking from the load. However, at the combiner output $V_2$, the open output of the main PA is transformed to a short circuit. The ESD amplifier outputs zero by absorbing the current from the filter into this short-circuit resonator. At "1" state, both devices are turned on and driven into voltage saturation. As the filter limits the output current to a value between zero and the maximum current $2I_{max}$, the equivalent impedance looking into the filter and the load is higher than $R_{opt}/2$, where the optimum impedance $R_{opt}$ is defined by $V_{max}/I_{max}$. The auxiliary PA forces the voltage at the combiner output $V_2$ to be $V_{max}$ as it sees a high impedance at the output which forces it to operate at the maximum output voltage. Therefore, it works like a RF voltage source with pulsed amplitudes, as shown in Fig. 3. This in turn forces the current output of the main PA to reach to the maximum because of current and voltage relations of the quarter wave impedance transformer given in (1).

$$V_1 = jR_{opt} I_m, \quad V_2 = jR_{opt} I_1 \tag{1}$$

To understand the efficiency performance of the ESD amplifier at different level of output power, a quasi-steady-state can be applied assuming the switching speed of envelope modulator is much greater than the bandwidth of high Q bandpass filter. In this assumption, the output current of PA is proportional to duty cycle of envelope modulator and stays constant during the full cycle. As described in Fig. 3, the effective output load during the turning on period, $R_{eff}$ can be defined using duty cycle $D$ and the equations are given in (2) and (3).

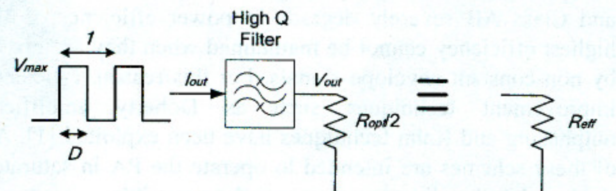


Fig. 3. Voltage source input upon a current filter and the equivalent load impedance model at quasi-steady-state.

$$\begin{cases} V_{out} = V_{max} D \\ I_{out} = \dfrac{V_{out}}{R_{opt}/2} = 2I_{max} D \end{cases} \tag{2}$$

$$R_{eff} = \frac{V_{max}}{I_{out}} = \frac{1}{D} \cdot R_{opt}/2 \tag{3}$$

The output power is given by (4) using (2).

$$P_{out} = \frac{1}{2} I_{out} V_{out} = I_{\max} V_{\max} D^2 \quad (4)$$

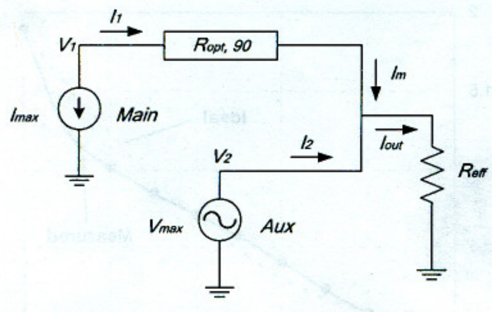


Fig. 4. Equivalent circuit model for quasi-steady-state ESD.

As the auxiliary PA goes into saturation for any $R_{eff}$ higher than $R_{opt}/2$, the auxiliary PA can be modeled as a voltage source ($V_{max}$) and from (1), the main PA can be modeled as a current source ($I_{max}$) (Fig. 4). Thus,

$$V_2 = V_{\max}, \quad I_1 = I_{\max} \quad (5)$$

When $0.5 < D < 1$, as $I_{out}$ becomes greater than $I_{max}$, the main PA provides the maximum possible current of $I_{max}$ and the auxiliary PA provides the remaining current as follows.

$$\begin{aligned} I_m &= I_{\max} \\ I_2 &= I_{out} - I_m = I_{\max}(2D-1) \\ V_1 &= V_{\max} \end{aligned} \quad (6)$$

DC power can be calculated using $\gamma$ which is the ratio between DC current and RF current ($\pi/2$ for Class B).

$$\begin{aligned} P_{DC} &= (I_{DC1} + I_{DC2})V_{DC} = (\gamma DI_1 + \gamma DI_2)V_{DC} \\ &= 2\gamma I_{\max} V_{\max} D^2 \end{aligned} \quad (7)$$

In addition, the drain efficiency is given by (8).

$$\eta = \frac{P_{out}}{P_{DC}} = \frac{1}{2\gamma} = \frac{\pi}{4} = 78.5\% \quad (8)$$

When $0 < D < 0.5$, $I_{out}$ is less than $I_{max}$ and all the current is provided by the main PA.

$$\begin{aligned} I_m &= 2I_{\max} D \\ I_2 &= 0 \\ V_1 &= I_1 R_{opt} = 2V_{\max} D \end{aligned} \quad (9)$$

$$\begin{aligned} P_{DC} &= (I_{DC1} + I_{DC2})V_{DC} = (\gamma DI_1 + \gamma DI_2)V_{DC} \\ &= \gamma I_{\max} V_{\max} D \end{aligned} \quad (10)$$

Since $P_{out}$ is proportional to $D^2$, the drain efficiency of this duty cycle range is twice that of the Class B efficiency with the same amount of power back-off as given by (11).

$$\eta = \frac{P_{out}}{P_{DC}} = \frac{1}{\gamma} D = \frac{\pi}{2} D \propto \sqrt{P_{out}} \quad (11)$$

Fig. 5 summarizes the above equations. The maximum efficiency is maintained for 0.5 < D <1.0 which corresponds to 6dB back-off. In Fig. 6, the efficiency performance is compared with classical Doherty amplifier. The flat efficiency until 6dB back-off is maintained for the ESD amplifier while the Doherty amplifier has an efficiency dip.

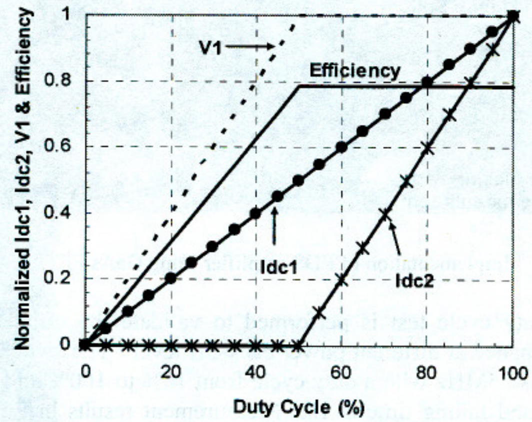


Fig. 5. Normalized DC currents, drain voltage and efficiency.

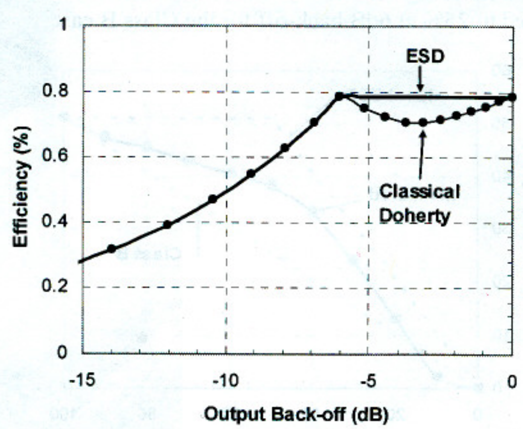


Fig. 6. Efficiency curve of ESD vs. classical Doherty Ampflier.

## III. Experimental Results

FLL351 GaAs FETs from Fujitsu are used to build Class B amplifiers at 1.87GHz. As shown in Fig. 7, RT/duroid is used for substrate and the amplifiers, microstrip splitter/combiner and the cavity filter are connected with SMA connectors with the insertion loss calibrated. For the output filter, a base station duplexer for PCS band is used which has about 30MHz bandwidth at the center frequency of 1.87GHz with an average passband insertion loss of 0.7dB. The stopband performance of the filter is also important beside the passband insertion loss. The stopband return should be almost complete reflective with relatively flat phase response over a certain bandwidth depending on the switching frequency. A 25 Ω T-line is added in front of filter to make sure that the phase of $S_{11}$ is close to zero degree to make an open circuit reflection.

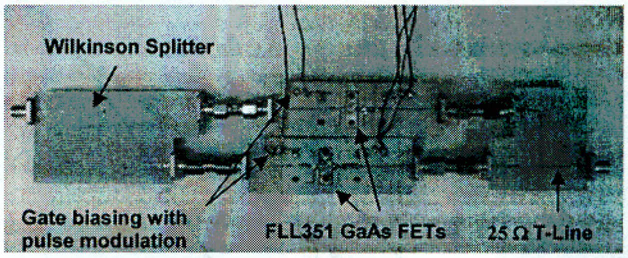


Fig. 7. Implementation of EDS amplifier using GaAs FETs.

A duty cycle test is performed to validate the efficiency performance at different power back-off level. The switching speed is 25MHz with a duty cycle from 10% to 100% and the rising and falling time is 1ns. Measurement results in Fig. 8 show similar efficiency behavior as predicted. The drain efficiency is about 50% at the full power and 38% at 6dB back-off including the cavity filter insertion loss. This is compared to 25% at 6dB back-off for the Class B case.

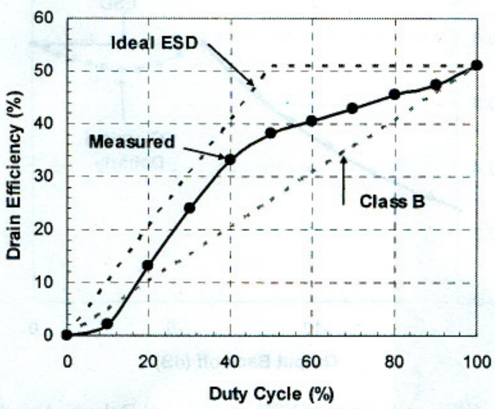


Fig. 8. Measured drain efficiency curve.

Measured output power for duty cycle is depicted in Fig. 9. Output power should be proportional to the square of the duty cycle to assure linearity. Deviation in the linearity curve is believed to be related to some loss in the gate switching drive circuitry, which is quite primitive in the current measurement setup.

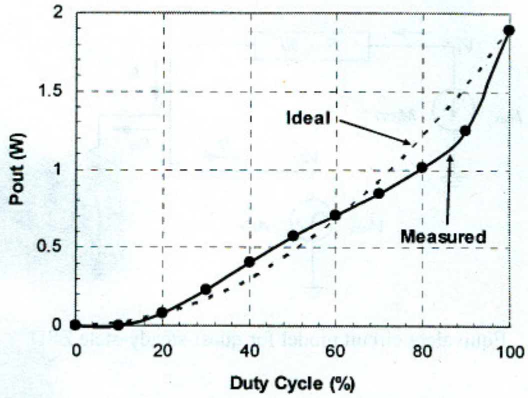


Fig. 9. Measured output power versus duty cycle curve.

## IV. Conclusions

The novel envelope switching Doherty amplifier with optimal efficiency over a wide range of output level is proposed. The amplifier is implemented with commercially available packaged GaAs FETs. The measured results have validated the proposed concept.


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